Claims 3, 4, 6, 7, 13, 15, and 16 were objected to as depending from rejected base claims. Reconsideration of the Claims is respectfully requested.

1. Rejection under 35 U.S.C. Section 103

In general, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Although the Supreme Court, in re-confirming the Graham factors, had admonished the use of the teaching-suggestion-motivation (TSM) test as an end of the obviousness inquiry, "[the Court] also recognized that [the teaching-suggestion-motivation (TSM) rationale] was one of a number of valid rationales that could be used to determine obviousness." MPEP § 2143 at 2100-118 (Rev. 6, Sept. 2007). Under this rationale, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Also, a finding is to be articulated that there was a reasonable expectation of success. MPEP § 2143 (G) at page 2100-138 (Rev. 6, Sept. 2007).

Further, all claim limitations must be considered. That is, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." MPEP § 2143.03 at page 2100-142 (Rev. 6, Sept. 2007) (citations omitted).

Claims 1-2, 5, 8, 11-12, 14, and 17-29 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,592,476, to Calamvokis et al. ("Calamvokis"), in view of U.S. Patent No. 7,020,141, to Stacey et al. ("Stacey").

Calamvokis relates to "apparatus for receiving at least one input stream of packets each having a packet body and multicasting this stream as a plurality of output streams by copying across the packet bodies . . . into packets of the output streams, the input and output streams being identified in the apparatus by input and output identifiers . . . ." (Calamvokis 3:62-67, to 4:1-2).

Calamvokis recites, with respect to its Figure 3, an "ATM switch:"

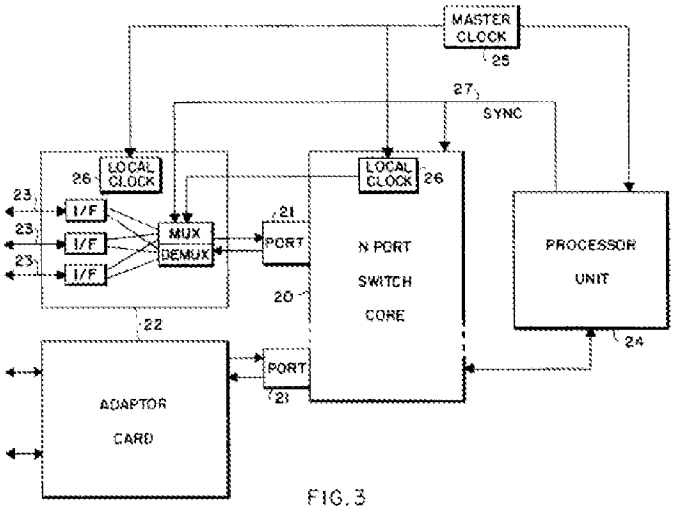
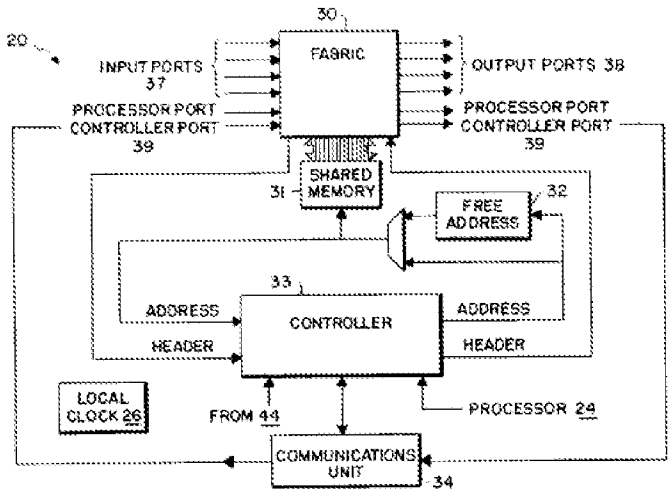


FIG. 3

(Calamvokis 6:6-7). The switch core block 20 is illustrated with respect to Figure 4 of Calamvokis:



In Figure 4 of Calamvokis, the N-part switch core 20 "comprises a switch fabric 30 with input and output ports 37, 38 which are generally paired and as such constitute the switch core ports, a shared cell-body memory 31, a free address list memory 32, a controller 33, and a communications block 34 for carrying out ATM adaption layer and other higher communication layers processing of cells intended for/coming from the controller (thereby enabling the latter to communicate over the network of which the switch forms a part)." (Calamvokis 7:37-46).

Calamvokis recites that in operation, the switch core 20 "input ports 37 are serviced in strict order one cell at a time. When a cell comes in on one of the input ports the Fabric 30 writes the cell body into the Shared Cell Body Memory 31 at an address taken from the free address list memory 32. This address is also passed to the Controller 33, along with the header of the cell to which it relates. Because the input ports 37 are serviced in a fixed order, the Controller 33 can tell the source of the cell from the arrival time of the header." (Calamvokis 7:47-56).

With respect to the controller 33, Calamvokis recites that it "stores and processes the headers and cell body addresses of incoming cells. It also makes decisions about which cell to send next on each output port 38 based on the queueing model and scheduling policies (to be described hereinafter). To send a cell the controller outputs the cell's header and the address at which the cell's body is stored. The fabric 30 reads the cell body out of the Shared Cell Body Memory 31, combines it with the header and sends the cell on an output port. *As the output ports are also serviced in a fixed order, the destination of the cell is determined by the time at which the controller sends the header and address*." (Calamvokis 7:57-64) (emphasis added).

That is, as understood, Calamvokis does not recite determining an output virtual channel for the data block, transferring the data block from the input virtual channel linked list of the receiver buffer to a destination within the host device via the output virtual channel; and updating the input virtual channel linked list to remove the data block. Instead, Calamvokis recites the destination of the cell is determine d by the time at which the controller sends the header and address.

Stacey relates to providing "an improved arrangement and method for providing functional partitioning of an ATM adaption layer [(AAL)]." (Stacey 2:22-24). Stacy recites that "such a partitioning [of AAL functionality into a number of key devices] separates the key functions of the system such that the divergent requirements of voice and data applications can be provided in specialised devices that are unencumbered with the orthogonal functionality necessary to support

the other service yet through the use of a common CPS layer still retains the ability to multiplex voice and data services together onto the same physical ATM link and (for AAL2) within the same VCC connection." (Stacey 4:38-46).

Referring to Figure 6, Stacey recites a "dynamic [Common Part Sublayer (CPS)] buffer architecture [that] is logically organised as a shared buffer together with associated control and pointers:" (Stacey 6:7-9). The queuing options are set out by the nature of the Virtual Channel, either on a "per incoming link queue," "per incoming (AAL2) VC queues," "per AAL2 connection queues," "per outgoing AAL2 VCC queues," or "per outgoing AAL2 VCC per priority." (Stacey 6:41-59). That is, as understood, Stacey does not update an input virtual channel linked list corresponding to the input virtual channel to include the data block, determine an output virtual channel for the data block, transfer the data block from the input virtual channel linked list to a destination within the host device via the output virtual channel.

Instead, Stacey, within its common part sublayer (CPS), recites that an SDU can be logically moved by transporting a pointer to the slot to the required process, based upon the queue order. (*see* Stacey 6:22-26). Further, in achieving an "optimized buffering apportionment in order to minimize the delay through any system," Stacey recites an optimal buffering "according to a shared memory output buffered paradigm. Such a paradigm is preferred over other potential buffer schemes in that it minimizes the overall sub-system delay, the memory requirements, the potential for blocking and the signal flow complexity." (Stacey 5:21-29; 2:14-18). That is, the paradigm, and not the queue structure (that is dissimilar to that recited in Applicant's Specification), is considered the aspect that increases the device efficiency.

Distinguishable from fixed-order output ports of Calamvokis and the overlapping memory buffer paradigm of Stacey, Applicant's Specification at page 3 notes that "servicing a *peripheral bus interconnection* requires significant processing and storage resources. . . . [Incoming] data may have been transmitted from a variety of source devices with data coming from the variety of source devices being interleaved and out of order. The receive port must organize and order the incoming data prior to routing the data to a destination resource within the serviced device or to a transmit port that couples to the peripheral bus fabric. The process of receiving, storing, organizing, and processing the incoming data is a daunting one that requires significant memory for data buffering and significant resources for processing the data to organize it and to determine an intended destination." (Specification at Page 3, *ll.* 3-16).

Applicant's Specification, at page 16, further recites that a "virtual channel may correspond to a particular physical entity, such as processing units 42-44, cache memory 46 and/or memory controller 48, and/or to a logical entity such as a particular algorithm being executed by one or more of the processing units 42-44, particular memory locations within cache memory 46 and/or particular memory locations within system memory accessible via the memory controller 48. In addition, one or more virtual channels may correspond to data packets received from downstream or upstream nodes that require forwarding. Accordingly, each multiple processor device supports a plurality of virtual channels. The data of the virtual channels, which is illustrated as data virtual channel #1 (VC#1), data virtual channel #2 (VC#2) through data virtual channel #n (VC#n) may have a generic format. The generic format may be 8-byte data words or 16-byte data words that correspond to a proprietary protocol, ATM cells, IP packets, TCP/IP packets, other packet switched protocols and/or circuit switched protocols." (Specification at p. 16, *ll.* 29-32 through p. 17, *ll.* 1-9).

In kind, Applicant's Independent Claim 1 recites, *inter alia*, a "method for routing data *within a host device* comprising: receiving a data block at a receiver of the host device . . . *updating an input virtual channel linked list corresponding to the input virtual channel to include the data block*; determining an output virtual channel for the data block; *transferring the data block from the input virtual channel linked list of the receiver buffer to a destination within the host device via the output virtual channel*; and *updating the input virtual channel linked list to remove the data block*." (emphasis added).

Applicant's Independent Claim 11 recites, *inter alia*, a "method for routing data *within a host device* comprising: . . . when the input virtual channel has identified therewith an output virtual channel updating an output virtual channel linked list corresponding to the output virtual channel to include the data block; and when the input virtual channel *has not identified therewith an output virtual channel*: updating an input virtual channel linked list corresponding to the input virtual channel to include the data block; *processing the data block to determine an output virtual channel* for the data block; updating an output virtual channel linked list corresponding to the output virtual channel to include the data block; and updating the input virtual channel linked list to remove the data block." (emphasis added).

Applicant's Claim 20 recites, *inter alia*, a "received *data processing and storage system* comprising: . . . a routing module that determines an output virtual channel for data blocks based

upon their respective input virtual channels; a receiver buffer operable to instantiate an input virtual channel linked list for storing data blocks *on an input virtual channel basis* and to instantiate *a free list that identifies free data locations*; a linked list control module operably coupled to the receiver buffer; input virtual channel linked list registers operably coupled to the linked list control module; and *free linked list registers* operably coupled to the linked list control module." (emphasis added).

In view of the above, Applicant respectfully submits that the fixed-order output ports of Calamvokis and the overlapping memory buffer paradigm of Stacey does not set forth "each and every element as set forth in [Applicant's claims]." Further, Applicant respectfully submits that there is no suggestion or motivation for the hypothetical combination of Calamvokis and Stacey to achieve Applicant's claimed invention.

2. Allowable Subject Matter

Applicant notes with appreciation the indication of allowability to Claims 3, 4, 6, 7, 13, 15, and 16, which would be allowable if rewritten in independent form.

3. Conclusion

As a result of the foregoing, the Applicant respectfully submits that claims 1-29 in the Application are in condition for allowance, and respectfully requests allowance of such Claims.

If any issues arise, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ksmith@texaspatents.com.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126.

Respectfully submitted,

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